[ENGLISH TRANSLATION]

Japanese Laid-open Patent
Laid-open Number: Hei 8-274336
Laid-open Date: October 18, 1996
Application Number: Hei 7-72675
Filing Date: March 30, 1995
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[Title of the Invention] Polycrystalline semiconductor thin film transistor and method of manufacturing the same

[Abstract] (Amendment)

[Object] To provide a thin film semiconductor field-effect transistor which has high current drive capacity, a small size element, and an LDD structure so as not to increase the number of manufacturing steps so much.

[Structure] In a coplanar MIS thin film transistor, a semiconductor layer 3 composed of polycrystalline silicon is formed as a channel region. In the transistor, a gate electrode 4_2 has a protrusion structure in which an area of the vicinity of a portion contacting with a gate oxide film 2 is larger than that on the opposite side, and the polycrystalline silicon layer 3 facing the electrode is doped with the same conductive type determining impurities as a source/drain in a less amount than the source/drain.

[Scope of Claims]

[Claim 1] A polycrystalline semiconductor thin film transistor,

transistor, comprising: a substrate having an insulating surface; a polycrystalline semiconductor layer which is formed on the substrate and has a channel region formed in an inside thereof; a gate insulating film formed on the polycrystalline semiconductor layer; a gate electrode formed on the gate insulating film; and source/drain regions formed in contact with both sides of or in the inside of the polycrystalline semiconductor layer, characterized in that the gate electrode is composed of: a first gate metal layer formed on a side closer to the gate oxide film; and a second gate metal layer which is formed on the first gate metal layer and is short in a gate length direction compared to the first gate metal layer.

[Claim 2] A polycrystalline semiconductor thin film transistor, comprising: a substrate having an insulating surface; a polycrystalline semiconductor layer which is formed on the substrate and has a channel region formed in an inside thereof; a gate insulating film formed on the polycrystalline semiconductor layer; a gate electrode formed on the gate insulating film; and source/drain regions formed in the inside of or in contact with both sides of the polycrystalline semiconductor layer, characterized in that: the gate electrode has a shape with a bottom being wide on a side closer to the gate oxide film; and an angle of the bottom with the substrate surface is 20° or less.

[Claim 3] A method of manufacturing a polycrystalline

semiconductor thin film transistor, characterized by comprising the steps of: forming a polycrystalline semiconductor layer on a substrate having an insulating surface; forming a gate insulating film on the polycrystalline semiconductor layer; forming a first gate metal layer on the gate insulating film on a side closer to the gate oxide film; forming a second gate metal layer which is formed on the first gate metal layer and is short in a gate length direction compared to the first gate metal layer; and performing impurity implantation from above the first and second gate metal layers to form source/drain regions on the polycrystalline semiconductor layer.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Application]

The present invention relates to a polycrystalline semiconductor thin film transistor.

[0002]

[Prior Art]

A thin film transistor (TFT) can be formed on a substrate that has a large area and varies in material, and is therefore expected to have a wide range of applications. In one of the largest fields of the recent applications, the TFT is applied to a switching element of a liquid crystal display device. Although the TFT in practical use is currently made by using amorphous silicon, since the

amorphous silicon has low mobility, there are problems in that an element size becomes large in order to perform large current switching, high speed switching cannot be performed, and the like. To provide a measure for solving these problems, it has been attempted to manufacture the TFT by using polycrystalline silicon for a channel. However, in the case of the TFT using the polycrystalline silicon, a leakage current is likely to occur due to electric field concentration in the vicinity of an end of a drain. Accordingly, for use in pixel switching, an LDD structure in which a low concentration impurity layer is formed in a part of the drain must be used to avoid the electric field concentration, thereby reducing the leakage current.

[0003]

Fig. 5 shows such a conventional LDD structure in order of manufacturing step. First, a polycrystalline silicon film is formed on a glass substrate 1 and processed into an island shape, on which a silicon oxide gate insulating film 43 is formed. Next, patterning is performed to form a gate electrode 45 of MoTa by a PEP (through which a predetermined portion of a resist is photosensed, a resist mask is then formed by removing an unnecessary portion, and etching is performed on this resist mask to process a layer under the resist) step. Thereafter, ion implantation is performed using the gate electrode 45 as a mask to form low concentration regions 46_1 and 47_1 (Fig. 5(a)).

[0004]

Subsequently, the second PEP is performed to form a pattern which is larger than a gate with a silicon oxide film 40. After that, P ion implantation is performed using this pattern as the mask to form high concentration regions 48 and 49 to serve as source/drain regions and also to form LDD regions 46_2 and 47_2 (Fig. 5(b)).

[0005]

Finally, opening portions are provided above the high concentration regions 48 and 49 in a surface protection film formed over the entire surface, and source/drain electrodes of Al are formed in these opening portions to complete the thin film transistor (Fig. 5(c)).

[0006]

In this method, a minimal size of the LDD regions 46_2 and 47_2 that can be formed is determined based on accuracy in two mask alignment steps. According to the current mask alignment accuracy, it is difficult to obtain the LDD region with a width of 2 μm or less. In addition, in the case of being formed on the glass substrate, the LDD region is reduced to only about 4 μm in width taking into account shrinkage of the substrate during processing. Thus, the LDD regions 46_2 and 47_2 become large and cannot be ignored as resistance components. As a result, sufficient current drive capacity has not been obtained. Also, it has been difficult to make

the element size smaller as long as the LDD regions 46_2 and 47_2 cannot be made smaller.

[0007]

[Problem to be solved by the Invention]

As described above, in a conventional LDD structure TFT using polycrystalline silicon, it is impossible to obtain an LDD region having an optimal width. Therefore, a conventional element has a large size and insufficient current drive capacity.

[0008]

The present invention has been made in view of the above problems. Therefore, an object of the present invention is to provide a polycrystalline semiconductor thin film transistor, in which an electrode structure is changed to thereby realize an improved drive capacity and a small size.

[0009]

[Means for solving the Problem]

According to Claim 1 of the present invention, there is provided a polycrystalline semiconductor thin film transistor, which includes: a substrate having an insulating surface; a polycrystalline semiconductor layer which is formed on the substrate and has a channel region formed in an inside thereof; a gate insulating film formed on the polycrystalline semiconductor layer; a gate electrode formed on the gate insulating film; and source/drain regions formed in contact with both sides of or in

the inside of the polycrystalline semiconductor layer, characterized in that the gate electrode is composed of: a first gate metal layer formed on a side closer to the gate oxide film; and a second gate metal layer which is formed on the first gate metal layer and is short in a gate length direction compared to the first gate metal layer.

[0010]

According to Claim 2 of the present invention, there is provided a polycrystalline semiconductor thin film transistor, which includes: a substrate having an insulating surface; a polycrystalline semiconductor layer which is formed on the substrate and has a channel region formed in an inside thereof; a gate insulating film formed on the polycrystalline semiconductor layer; a gate electrode formed on the gate insulating film; and source/drain regions formed in the inside of or in contact with both sides of the polycrystalline semiconductor layer, characterized in that: the gate electrode has a shape with a bottom being wide on a side closer to the gate oxide film; and an angle of the bottom with the substrate surface is 20° or less.

[0011]

According to Claim 3 of the present invention, there is provided a method of manufacturing a polycrystalline semiconductor thin film transistor, characterized by including the steps of: forming a polycrystalline semiconductor layer on a substrate having

an insulating surface; forming a gate insulating film on the polycrystalline semiconductor layer; forming a first gate metal layer on the gate insulating film on a side closer to the gate oxide film; forming a second gate metal layer which is formed on the first gate metal layer and is short in a gate length direction compared to the first gate metal layer; and performing impurity implantation from above the first and second gate metal layers to form source/drain regions on the polycrystalline semiconductor layer.

[0012]

Here, it is desirable in view of improvement of element speed that the gate electrode be formed of a conductor having two layers or more and the closer layer to the gate insulating film have the lower resistance. Also, it is preferable in view of reliability in element characteristics that the polycrystalline semiconductor be of polycrystalline silicon.

[0013]

Further, it is desirable in view of reduction of a leakage current that the angle of the bottom of the gate electrode with the substrate surface be 20° or less. Also, it is desirable in view of the reduced leakage current that the bottom of the gate electrode, or a protrusion of the first gate metal layer from the second gate metal layer in the gate length direction, be 0.2 μm or more.

[0014]

Furthermore, it is desirable in view of obtaining an LDD

structure with excellent characteristics that, in the polycrystalline semiconductor layer, impurities under the gate electrode be the same conductive type determining impurities as the source/drain regions of the polycrystalline semiconductor thin film transistor and a concentration thereof be equal to or lower than a tenth of the impurity concentration of the source/drain regions.

[0015]

[Operation]

According to the above-described structure, under a protrusion of the first gate metal layer from the second gate metal layer in the gate length direction, or the bottom of the gate electrode, there is formed a low impurity concentration layer which has a low impurity concentration and is shorter in the gate length direction compared to a conventional structure. Thus, since the low impurity concentration layer is short, the LDD structure having a low resistance is accurately formed, whereby the polycrystalline semiconductor thin film transistor can be provided in which an improved drive capacity and a smaller size are realized.

[0016]

[Embodiment]

The present invention will be described in detail with reference to embodiments.

(Embodiment 1)

Embodiment 1 of the present invention will be described with reference to sectional views in order of manufacturing step shown in Fig. 1 and Fig. 2.

[0017]

First, a quartz substrate 1 is used and an amorphous Si layer is formed on this substrate 1 by a CVD method. Then, annealing is performed at 600°C for 20 hours, to form a polycrystalline Si layer 2 having a thickness of 50 nm. Although not shown here, this polycrystalline Si layer 2 is processed into an island shape in order to be electrically separated from another polycrystalline Si layer on the quartz substrate 1, followed by which an SiO_2 layer 3 is formed to a thickness of 70 nm by an atmospheric pressure CVD method. After that, as gate electrode materials, a tungsten layer 4_1 is formed to a thickness of 20 nm and a molybdenum layer 5_1 is formed to a thickness of 100 nm. After that, a resist 6_1 is adhered to a portion to be left as a gate electrode (Fig. 1(a)).

[0018]

Thereafter, the gate electrode materials are etched by an RIE method which uses oxygen and fluoride gases to form a tungsten layer 4_2 and a molybdenum layer 5_2. At this time, a proportion of oxygen is first lowered to perform etching under a condition that a width of the layers is similar to that of the resist 6_1 (Fig. 1(b)).

[0019]

Thereafter, oxygen concentration is raised to continue the

etching under the condition that the resist 6_1 is also etched, whereby the width of the resist becomes smaller and a metal 5_3 just under a resist 6_2 is also subjected to the etching. Although the gate electrode may be completed here, the etching can be further continued to form a shape having a clearly wide bottom (Fig. 1(c)).

[0020]

That is, the gases are replaced to further etch the metal in an upper layer under the condition that a metal in a lower layer is not etched. After that, removing the resist provides a gate with such a structure that a metal 5_4 in the upper layer is narrower than a metal 4_2 in the lower layer. In this manner, there are formed the tungsten layer 4_2 serving as a first gate metal, and a molybdenum layer 5_4 as a second gate metal layer which is shorter than the tungsten layer 4_2 in a gate length direction. In this case, it is also possible to express the gate electrode as having a two-stairstep shape (Fig. 1(d)).

[0021]

Thereafter, using an ion implantation apparatus in which mass separation is not performed (ion doping apparatus), ion implantation is performed with P ions under the condition of 100 keV and 3 x $10^{13}/cm^2$ to form low impurity concentration layers 6_1 and 7_1 (Fig. 2(a)).

[0022]

Thereafter, the ion implantation is performed under the

condition of 50 keV and 3 x $10^{15}/cm^2$ to form high impurity concentration source/drain regions 8 and 9 and also to form low impurity concentration layers 6_2 and 7_2 (Fig. 2(b)).

[0023]

Thereafter, an interlayer insulating SiO_2 film 14 is adhered and a contact hole is formed, followed by which Al electrodes 10 and 11 are adhered and formed to obtain source/drain electrodes 10 and 11.

[0024]

Thereafter, although not shown, a passivation film or the like is formed over the entire surface to complete a thin film field-effect transistor. Fig. 3 shows a study result of a relationship (indicated by a solid line) between a gate voltage and a drain current of the thin film field-effect transistor in the above embodiment, and also shows, for comparison, a relationship (indicated by a broken line) between the gate voltage and the drain current of a conventional thin film field-effect transistor with an LDD structure. As is apparent from this figure, in the TFT of this embodiment, it is possible to improve an ON current compared to the conventional TFT.

[0025]

In this manner, by using the present invention, it becomes possible to produce the thin film field-effect transistor with high current drive capacity. In addition, since the low impurity

concentration layer is formed in a self-aligning manner with the gate electrode, there occurs no misalignment of the mask due to a PEP step, allowing the thin film field-effect transistor to have stable characteristics and improving a yield. Also, in the case of application to a driver circuit TFT of a liquid crystal display device which is obtained by forming and integrating a pixel electrode, a switching TFT for the pixel electrode, a driver circuit, and the like on an insulating substrate, there is considerable complexity with a conventional method since the driver circuit and a pixel switch differs in structure of the thin film field-effect transistor. However, the driver circuit and the pixel switch are allowed to have the same structures with the present method, to make the circuit design much simpler. Also, the current drive capacity of a pixel switching MIS field-effect transistor becomes higher, whereby an occupied area which the transistor occupies on the insulating substrate can be made smaller. That is, for example, the occupied area of 10 x 10 μm/□ occupied by the conventional thin film field-effect transistor can be reduced to that of 7 x 10 μm/□ occupied by the transistor of this embodiment, making it possible to realize a smaller size element. At the same time, a leakage current also becomes smaller, thereby enabling to reduce an auxiliary capacitance and to raise an aperture ratio.

(Embodiment 2)

Fig. 4 is a sectional view of the thin film field-effect

transistor showing Embodiment 2 of the present invention. According to the present method, when a metal layer is etched to form the gate electrode, it is possible to produce a gate electrode shape of the present invention at one time by selecting an etching condition. As is the same in Embodiment 1, in the case of Embodiment 2, a side surface of a gate electrode 35 has a bottom 36 having a slanting shape and a sectional surface of the gate electrode 35 has the shape close to an L-form overall, and it is found that: it is preferable that a protrusion of the bottom of the gate electrode from a top portion of the gate electrode be more than 0.2 μm in the gate length direction; and it is also desirable that a broadening angle of the bottom be 20° or less with respect to a substrate surface. A reason for this is as follows. That is, even when an ordinary etching is performed, the side surface of the gate is slanted. However, a slanting angle thereof, which is standing, indicates the shape at 45° or more with respect to the substrate 1. However, with such a shape, even if an ion accelerating voltage is changed, there is formed almost no LDD region, and therefore, a reverse direction leakage of a MIS does not reduced. In an experiment by the present inventors, in the case of a protruding portion being 0.5 μm or 0.3 μm in length, when produced at an angle with the substrate of 5°, a MIS transistor having the most preferable characteristics was obtained. In order to form LDD regions until electric characteristics are improved, it is desirable that the

bottom 36 of the gate electrode have an angle of approximately 5° with respect to the substrate surface. In our experiment, even when the angle was increased to 20°, improvement of the characteristics was observed. Thus, it was found that, in the case of the angle being 20° or less and the protruding portion being 0.3 μm in length, the LDD structure can be produced by one PEP step. When the angle with the substrate was 0° and the protruding portion was 0.5 μm in length, exactly the same effect as in Embodiment 1 was obtained.

[0026]

The present invention is not limited to the above embodiments, and the intention thereof may be put into practice through various modifications. In the above-described embodiments of the present invention, used as a conductive layer closer to a gate insulating film in the gate electrode is polycrystalline silicon, and used as a portion farther from the gate insulating film is a metal such as tungsten, molybdenum, chromium, titanium, platinum, vanadium, nickel, aluminum, copper, gold, silver, palladium, niobium, or tantalum. In this case, a channel and the gate electrode which is in contact with an oxide film are made of the same material, and a threshold value of the MIS transistor can be prevented from changing due to a difference in work function between substances.

[0027]

Also, as the gate electrode of the above-described embodiment, there can be used a combination of: alloys or compounds among mutual

metals selected from the group consisting of tungsten, molybdenum, chromium, titanium, platinum, vanadium, nickel, aluminum, copper, gold, silver, palladium, niobium, tantalum, and the like; or these metals or the alloys which are added minutely with beryllium, magnesium, calcium, zinc, cadmium, mercury, or other element. Such an alloy or a metal which includes a minute amount of impurities is preferable because etching rate thereof can be changed with ease depending on a composition ratio, and thus can produce such a shape as in the present invention.

[0028]

The polycrystalline semiconductor layer is not limited to silicon, but may also be another group IV semiconductor or compound semiconductor, for example, SiGe, SiC, or the like. Also, although impurity doping is not performed to the channel in the above embodiment, the doping to the channel may be performed to form a p-type or n-type field-effect transistor, which does not depart from the scope of the present invention.

[0029]

Also, the substrate having an insulating surface is not limited to a glass substrate, but may be the substrate as long as it is one having the insulating surface such as an SOI substrate. It is possible to use other various modifications.

[0030]

[Effect of the Invention]

By using the present invention, the polycrystalline semiconductor thin film transistor can be provided in which an improved drive capacity and a smaller size are realized.

[Brief Description of the Drawings]

[Fig. 1] A sectional view of a MIS TFT transistor in accordance with Embodiment 1 of the present invention.

[Fig. 2] A sectional view of the MIS TFT transistor in accordance with Embodiment 1 of the present invention.

[Fig. 3] A sectional view of the MIS TFT transistor in accordance with Embodiment 1 of the present invention.

[Fig. 4] A sectional view of a MIS TFT transistor in accordance with Embodiment 2 of the present invention.

[Fig. 5] A sectional view of a MIS TFT transistor having an LDD structure with a conventional method.

[Description of Reference Numerals]

1 insulating substrate

2 gate insulating film

3 polycrystalline silicon layer without doping

4 first gate metal layer

5 second gate metal layer

6, 7 polycrystalline silicon layer doped with low concentration impurity

8, 9 polycrystalline silicon layer doped with high concentration impurity

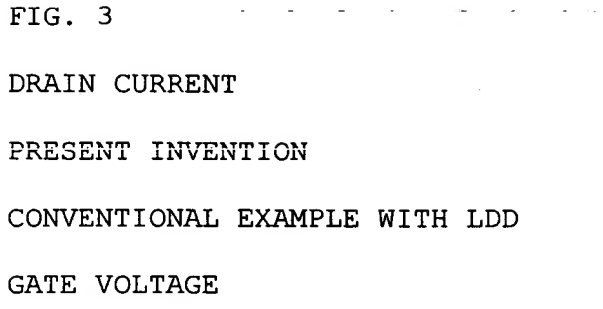
10 source electrode

11 drain electrode

14 insulating film

16 resist layer

FIG. 3


DRAIN CURRENT
PRESENT INVENTION
CONVENTIONAL EXAMPLE WITH LDD
GATE VOLTAGE